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09/836375
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Subclass	ISSUE CLASSIFICATION
Class	

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.
SCANNED Q.A.

PATENT DATE

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/836375	D	713	500	~~2182~~ 2115	Suryawanshi Lee

APPLICANTS: Peter Cook
Stanley Schuster

TITLE: Latch structure for interlocked pipelined CMOS (IPCMOS) circuits

PTO-2040 12/93

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ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	(Primary Examiner) (Date)			ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ___ months of this patent have been disclaimed.	(Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER	

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